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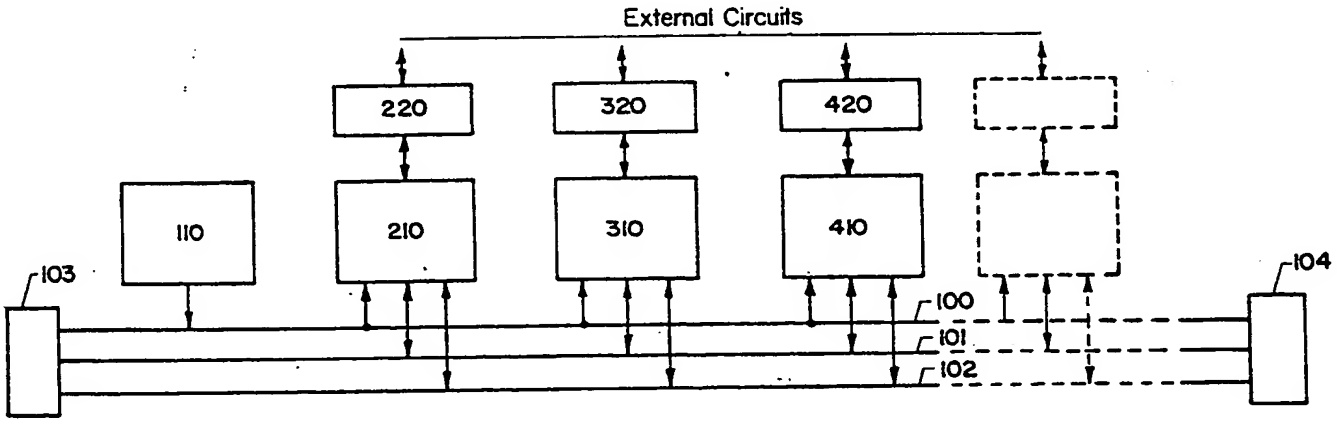

(57) Abstract

An electronic switching system using digital sampling and time division multiplexing to provide virtual connections between a plurality of external circuits. Each external circuit is connected to the matrix switch via respective line interface units (220, 320, 420). The conditioned external circuit signals are sampled by switch modules (210, 310, 410) and the time sampled information is exchanged between switch modules (210, 310, 410) via two switch buses (101, 102) under the control of a timing and control unit (110). Information transferred between switch modules (210, 310, 410) is synchronised to a cyclic time interval count generated by the timing and control module (110) and present on a control bus (100). Information transfers between external circuits are transparent to the switching system and its control unit.

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VIRTUAL BUS SWITCHING SYSTEM

The present invention relates to a digital switching system which performs the Matrix Switch function for Circuit Switching applications.

BACKGROUND ART

A Matrix Switch or Crosspoint Switch is a device used in a Space Division Switching System to enable any two or more attached circuits to be interconnected as required. A Space Division Switching System normally has a large number of electrical conductors or circuits terminating at a Matrix or Crosspoint Switch. By selectively connecting one or more switching nodes or crosspoints of the Matrix Switch an electrical connection is established between any two of these circuits.

The most common example of a Space Division Switching System is the analogue telephone exchange where a Matrix or Crosspoint Switch is used to interconnect subscriber telephones to each other on an "as requested" basis. A data communications switching system example is the requirement for a number of terminal devices to be able to be connected to more than one communications channel or host computer.

Most currently available circuit switching systems

implement a physical connection between two attached devices. This is accomplished by mechanical switches and relays or by electronic circuits. Circuit switching systems are normally arranged as a Switch Matrix enabling two or more circuits attached to the matrix to be physically and/or electrically connected via the Switch Matrix. This type of switching system establishes a permanent circuit through the switching system for the duration of the connection.

As the number of individual circuit connections increases the size of the Switch Matrix expands as a power function, which rapidly escalates the equipment size and cost. A 4x4 matrix switch, which can connect any two of the eight circuits, requires 16 individual switching nodes or crosspoints while a 32x32 matrix requires 1024 switching nodes. Each switching node may be required to connect more than one signal line for each circuit connection thus, the number of actual switching circuits can be very large for even a small number of circuit connections. In addition, the signal paths need not be symmetric, which further complicates the matrix if unidirectional electronic switching is used.

In recent years techniques such as Serial Time Division Multiplexing and Message Switching have been used to reduce the complexity of switching systems. These switching systems rely on the Switch Control having some knowledge of the information being passed between the connected devices.

These types of switching systems provide a significant reduction in the amount of physical hardware required to perform the switching function. However, as all information passing through the switching system has to be processed by the Switch Control, a fully information transparent switching function cannot be implemented.

SUMMARY OF THE INVENTION

It is the object of the present invention to provide

the information transparent, circuit switching function of a Space Division switching system at a size and cost more comparable to that of a Time Division or Message switching system.

The present invention differs from current switching system implementations in that it provides both matrix circuit switching and information transparency without requiring a large number of physical switching nodes or crosspoints.

According to the present invention there is provided a Virtual Matrix Electronic Switch which implements the circuit switching function of electrical signals present on electrical circuit conductors terminating at the Matrix Switch.

The majority of switching systems are used to route low information bandwidth signals and are therefore very amenable to the use of high speed sampling and multiplexing techniques to enable a number of low information bandwidth channels to efficiently share a high bandwidth channel with negligible loss of information content.

Whereas the circuit switching function in current Space Division switching systems establishes a permanent circuit connection between two terminating electrical conductors, the present invention employs the said high speed sampling and multiplexing techniques to achieve the same switching function without the requirement of a permanent circuit.

DESCRIPTION OF THE PREFERRED EMBODIMENT

In the preferred embodiment of the invention the electrical signals are preconditioned to appropriate signal levels before being switched. If the incoming signal is of an analogue type it is first converted to a digital representation at a sample rate consistent with maintaining the original information content. The conversion of analogue type signals to a digital format is not a

precondition of the invention, as appropriate sample and hold techniques would allow the signals to be switched as amplitude varying discrete samples of the analogue signal.

The preferred embodiment consists of one Timing and Control Module and a number of Switch Modules interconnected by three, multiple conductor, parallel signal Buses. Two of the Buses, known as the Switch Buses, are used to transfer information between Switch Modules installed in the system. The third bus, known as the Control Bus, is used by the Timing and Control Module to provide system timing and control signals to all Switch Modules.

The Timing and Control Module can include a Keyboard and Display Unit, or have an attached interactive terminal device, such as a CRT display, to allow direct operator control of the circuit connections. Alternatively, the circuit connection request can be provided by the attached device, such as a telephone handset.

Associated with each Switch Module is a Line Interface Unit which provides the demarcation between the switching system and attached external circuit. The Line Interface Unit provides the conversion between the electrical, or other types of signals, used by the attached devices and the electrical signals processed by the switching system.

The Switch Modules perform the actual switch function and exchange information via the Switch Buses. The two Switch Buses are equally accessible to each Switch Module installed in the system. Access by a Switch Module to the Switch Buses is determined by the Timing and Control Module. Binary encoded timing signals are generated by the Timing and Control Module and are monitored by each Switch Module.

The switching system's basic time period is known as the Transfer Slot period and is the time period required for two Switch Modules to execute an information exchange on the

Switch Buses. The timing section of the Timing and Control Module generates the Transfer Slot count which is received by all Switch Modules. The Transfer Slot count is cyclic and the time taken to increment through every Transfer Slot is known as the Transfer Slot Rotation period. As the Transfer Slot Rotation period, and hence the basic interface sample rate, depends on the total number of Transfer Slots, a smaller number of Transfer Slots provides a faster external circuit sample rate and vice versa. The minimum number of external circuit connections active at any one time is equal to the number of Transfer Slots in the Transfer Slot Rotation period. The Transfer Slot period is normally a fixed system parameter dependant on the physical implementation of the system switching circuits. The number of individual Transfer Slots and hence the Transfer Slot Rotation time can be a fixed or variable system parameter as required.

The Timing and Control Module allocates a Transfer Slot time and Switch Bus selection to each active Switch Module. Each Switch Module monitors the Transfer Slot count signals on the Timing and Control Bus. When the Transfer Time Slot value matches the allocated Slot number the Switch Module outputs the current state of the input signals present at its Line Interface Unit onto the allocated Switch Bus. At the same time it transfers the information present on the other Switch Bus to its Line Interface Unit. As Switch Modules are normally paired for any one Transfer Slot, the same procedure occurs at the other Switch Module, with the exception that the alternate Switch Buses are used for input and output. The information representing the instantaneous external circuit signals at the inputs of the pair of communicating Switch Modules are transferred to the outputs of the alternate Switch Module of the pair.

At the time of transfer between any two Switch Modules there is a circuit established between the two

modules via the Switch Buses. Information transfers occur simultaneously between both Switch Modules. When the Transfer Slot count changes to the next Transfer Slot period both Switch Modules release the Switch Buses, which then become available to Switch Modules that have been allocated the next Transfer Slot.

The Timing and Control Module communicates with each Switch Module via the Control Bus and can allocate each individual Switch Module a specific Transfer Slot time and the Switch Buses to be used for input and output.

As the Timing and Control Module allocates the Transfer Slot times for all Switch Modules it ensures that for any one Transfer Slot time only one pair of Switch Modules will have access to the Switch Buses. The Transfer Slot time and Switch Bus allocations are not specific to any individual Switch Module and are allocated as required.

The Switch Modules involved in a transfer have no synchronisation or interaction with each other except for the recognition of a valid Transfer Slot count.

The Line Interface Units convert the data received from the Switch Module into the form required by the external signal circuits. For a digital circuit the signals are converted to the appropriate digital levels while for an analogue circuit a digital to analogue conversion is performed and the resulting time continuous signal is conditioned to the required bandwidth and signal level.

The Switch Buses form part of the switching system and are normally an integral part of the Matrix Switch Printed Circuit backplane. The design of the Switch Bus backplane depends on the logic family used to implement the system. Each signal conductor of the Switch Bus is terminated at its characteristic impedance to minimise signal noise and cross coupling.

The information bandwidth of a Switch Buses during a Transfer Slot period is related to the number of parallel

signal paths making up the Switch Bus. The preferred embodiment has eight parallel signal paths for each Switch Bus however, this is not a restriction on the Matrix Switch architecture as the Switch Buses can be extended to any number of parallel signal paths required.

Each Switch Module in the Matrix Switch is identical and can occupy any position on the Switch and Control Buses. A Switch Module position is known to the Timing and Control Module by a unique address which, in turn, is the address of the corresponding external circuit. As all information transfers through the Matrix Switch are symmetric, any two external circuits can be interconnected via their corresponding Switch Modules. Allocation of the same Transfer Slot time to any two Switch Modules in the system initiates a virtual connection between their associated external circuits.

As can be determined from the preferred embodiment of the invention, the two Switch Modules operating in synchronism via the Switch Buses perform a high speed digital sample of their respective external circuits. The data is then transferred between the two Switch Modules to their outputs and held for one Transfer Slot Rotation period. As the output signals are time sampled replicates of the input signals the transfer is completely transparent to the Switch Modules and the system Timing and Control Module.

When the Matrix Switch is considered at the Line Interface Module inputs and outputs the transfer function is very similar to a permanent connection system. The switching transfer function does have an amount of non-cumulative error introduced due to the sampling function, which is directly related to the Transfer Slot rotation period. The number of external circuit connections that can be supported by the Switch Matrix at any one time is bounded by the sampling error tolerance of the external circuit and

its attached device.

The Transfer Time Slot Count is sequenced at a high rate, typically Megahertz. In data communications systems the rate of binary information change on any one signal line is relatively slow, typically up to 20 Kilobits/second while the analogue to digital conversion rate for telephone quality speech is 8000 conversions/second.

If the switching requirement for telephone quality speech is considered, the maximum period between successive sample is 125 microseconds. As the Matrix Switch can transfer the resulting binary word between Switch Modules in one Transfer Slot time the maximum Transfer Slot Rotation period is also 125 microseconds. If a typical Transfer Slot period of 100 nanoseconds, is assumed then the maximum number of Transfer Slots in one Transfer Slot Rotation period, or alternatively, the maximum number of active external circuit connections possible at any one time, is 1250.

The preferred embodiment demonstrates a switching system whereby the information transfers between external circuits are symmetrical and bidirectional. This is not a limiting factor of the invention and other arrangements such as asymmetrical switching or unidirectional switching to one or more external circuits from a single external circuit are within the scope of the invention.

In addition to providing external circuit connections via the Matrix Switch a suitable Timing and Control Module could be programmed to handle a number of higher level system functions not associated with the present invention's basic switching function.

These functions could include the prevention of incompatible circuits being connected, external circuit loopback, and test message generation and checking which can all be easily incorporated into the basic switching system architecture of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1. is a schematic block diagram of a limited Virtual Matrix Electronic Switching System according to the preferred embodiment of the present invention.

Figure 2. is a schematic block diagram of the Timing and Control Module of the system of Figure 1.

Figure 3. is a schematic block diagram of the Switch Module of the system of Figure 1.

Figure 4. is a schematic block diagram of a typical digital Line Interface Unit.

DETAILED DESCRIPTION OF THE DRAWINGS

In Fig 1. the switching systems three buses are shown. Bus 100 is the control bus which is the primary system bus and is used by the timing and control module 110 to distribute commands and timing information to switch modules 210, 310, 410 Buses 101 and 102 are the two switch buses used by the switch modules for the exchange of external circuit information. Each signal conductor of each bus is terminated in its characteristic impedance by terminating resistors 103 and 104 to minimise signal reflections during a bus operation. Each switch module is connected to the control bus and both switch buses and can receive or transmit information on either switch bus. Line interface units 220, 320, 420 provide the physical and electrical interface between switch modules and the external circuits. The line interface units also provide signal conditioning, conversion, isolation and medium translation, such as optical to electrical, if required.

Fig 2. shows detail of the timing and control module (110). A microcomputer (111) is used to provide the system management functions including the allocation of switch module transfer slot periods and switch bus selection. The microcomputer would normally be a single chip device however any implementation of a stored program computer which can perform the required functions is applicable. The

microcomputer connects to the control bus via a bus interface (112) which provides appropriate buffering of the bus signals. The timing generator (113) provides the basic system timing signals and the transfer slot count used by the switch modules to accurately synchronise information transfers on the switch buses. The timing generator also connects to the control bus via the bus interface. The control interface (114) is the user interface to the switching system to establish the required external circuit connections. The parameters can be provided directly to the switching system via a keyboard or terminal device. Alternatively, the request for an external circuit connection can be derived from the external circuits themselves with appropriate signal detection circuits, normally incorporated into the line interface unit.

Fig 3. shows detail of the switch module. The Transfer Slot latch (211) is accessible to the timing and control microprocessor and holds the Transfer Slot and the switch buses allocations to be used by the Switch Module for an information transfer. The timing decode logic (212) continuously monitors the Transfer Slot count on the control bus and compares it with the allocated value held in the Transfer Slot latch. When a match is detected the timing decode logic activates the bus switch control logic (213). The switch input latch (219) is closed, freezing the instantaneous value of the external circuit information in the latch for the duration of the transfer. An information transfer is then executed on the allocated Switch Buses. If, for example, switch bus 101 has been allocated as the switch module output bus then the switch bus control enables bus receiver 215 and bus driver 217. If switch bus 102 has been allocated as the output bus then bus receiver 214 and bus driver 216 are enabled. The transfer procedure is identical in both cases except for the switch buses used in the transfer. Using the first example; the external circuit

information held in latch 219 is output onto switch bus 101 via bus driver 217. At the same time bus receiver 215 allows information on switch bus 102 to pass to the inputs of latch 218. Near the end of the Transfer Slot period the information on Switch Bus 102 is stable and latch 218 is clocked updating the external circuit information at the line interface unit to the current time sampled value. At the end of the Transfer Slot period the timing decode logic deactivates the bus switch control and the switch module is disconnected from the switch buses.

The function of the line interface unit can vary depending on the signal type and transmission medium used for the external circuits. A typical line interface unit for digital signals is shown on Fig 4. Signal level translators and conditioners 221 and 222 perform the signal conversion between the external circuit signal levels and the switch module signal levels. The line interface unit would normally provide the physical connection (223) to the external circuits. Other types of line interface units could include analogue to digital and digital to analogue converters, optical to electrical and electrical to optical converters or other transmission medium or signal conditioning and conversion functions as required.

It should be understood that the present invention is to be given a broad connotation and it is not intended that it be restricted to the embodiment disclosed.

CLAIMS

1. A virtual matrix electronic switching system for providing the switching of information between a plurality of external signal circuits, said system comprising a plurality of electrical circuit interface and electrical signal conditioning means (220,320,420), a plurality of switching means (210,310,410) and a timing and control means (110), the said switching and timing and control means all being attached to a control bus (100) having a plurality of signal conductors, and each switching means (210,310,410) being attached to two information buses (101,102) each with a plurality of signal conductors, whereby each said switching means (210,310,410), under the control of the timing and control means (110), is able to transfer information from its associated external circuit to another external circuit associated with a like switching means (210,310,410), and simultaneously receive information from the external circuit associated with the like switching means (210,310,410) for transfer to its associated external circuit, such information transfers being the value of the external circuit information, or a representation thereof, at or near the time of the information transfer between like switching means (210,310,410), such transfers taking place on the said information transmission buses (101,102) as determined by timing and control signals presented on the said control bus (100) by the said timing and control means (110), whereby each and every switching means (210,310,410) is able to transfer information to another switching means (210,310,410) for a discrete time interval on a cyclic and periodic basis such that for any complete cyclic period a number of allocated switching means (210,310,410) have access to the said switch buses (101,102) for a discrete time interval to transfer external circuit information, if such a transfer is requested by the external circuit or other requesting means, and the said time interval

allocations can be changed by the timing and control means (110) in such a manner that any two switching means (210,310,410) may be logically connected for the said discrete time interval for the transfer of external circuit information, the said logical connection being also a logical connection between the two external circuits associated with the said two switching means (210,310,410).

2. A switching system as claimed in claim 1. wherein information present on external circuits attached to a switch module (210,310,410) via a line interface unit (220,320,420) is sampled at a periodic and cyclic rate, and such samples of the external circuit time continuous information, or a representation thereof, is transferred to a like switch module (210,310,410) during a defined time interval such that two communicating switch modules (210,310,410) proceed with a simultaneous, bidirectional information transfer via two switch buses (101,102), such transfers being determined by timing and control signals being generated by a timing and control module (110) and available to all switch modules (210,310,410) whereby such timing and control signals, and a predetermined timing interval allocation known to each switch module (210,310,410), being the only timing and control information required by a switch module (210,310,410) for the execution of an information transfer such that for any one timing interval only two switch modules (210,310,410) are enabled to exchange external circuit information with such transfers being at a high periodic rate whereby the time averaged value of the sampled external circuit information received by a switch module (210,310,410), and transferred to the destination external circuit via its associated line interface unit (220,320,420), closely approximates the actual time continuous external circuit information of the source external circuit.

3. A switching system as claimed in claim 2.

whereby the control of the transfer of external circuit information by a switch module (210,310,410) is determined by timing and control signals generated by the timing and control module (110), such timing and control signals define a specific timing interval rotation period which is subdivided into the timing intervals used by the said switch modules (210,310,410) for the transfer of external circuit information and the said timing interval rotation period is cyclic such that during any arbitrary long period of time there will occur a number of timing interval rotation periods that are further subdivided into into a number of transfer timing intervals which are repeated on a cyclic basis.

4. A switching system as claimed in claim 3. wherein the transmission medium for the timing and the transfer of the time sampled external circuit information consists of multiple conductor buses (100,101,102) constructed on a printed circuit backplane, with the said buses (100,101,102) being terminated in their electrical characteristic impedances (103,104), and such buses (100,101,102) are used by the timing and control module (110) and all switch modules (210,310,410) to transfer time sampled external circuit information between like switch modules (210,310,410), such transfers requiring only the recognition of a designated timing interval as is continuously incremented by the timing and control module (110) being the timing interval previously allocated to a switch module (210,310,410) by the timing and control module (110) such that each switch module (210,310,410) is able to execute an information transfer independantly of any other switch module (210,310,410) except for the external circuit information received from the switch bus during an information transfer time interval.

5. A switching system as claimed in claim 4. wherein each switch module (210,310,410) is able to access

equally each of the two switch buses (101,102) for the transmission and reception of external circuit information, the switch bus selection for the information transfer being predetermined by the timing and control module (110) and allocated to the switch module (210,310,410) such that for two communicating switch modules (210,310,410) the switch bus (101,102) allocated to one switch module (210,310,410) for the transmission of external circuit information is used by the other switch module (210,310,410) for the reception of the transmitted external circuit information, and vice versa, such that during during the transfer timing interval external circuit information is simultaneously transferred between the two communicating switch modules (210,310,410).

6. A switching system as claimed in claim 5. whereby under the control of the timing and control module (110) any switch module (210,310,410) can be instructed to transfer external circuit information during any predetermined timing interval, such timing intervals being provided to all switch modules (210,310,410) on the control bus (110), and during the said predetermined timing interval a switch module (210,310,410) will transmit its external circuit information and receive other external circuit information on the two switch buses (101,102) and such allocation of the switch buses (101,102) to be used by a switch module (210,310,410) for the transmission and reception of external circuit information can be changed at any time by the timing and control module (110), such changes to the timing interval and switch bus allocation for any one of the switch modules (210,310,410) will enable the timing and control module (110) to command any two switch modules (210,310,410) to exchange external circuit information and such an exchange will form a logical connection between the external circuits associated with the said two switch modules (210,310,410) for the duration of the timing interval during which the information exchange

takes place and the said information exchange is transparent to the operation of the switching system.

7. A switching system as claimed in claim 6. wherein the simultaneous transfer of time sampled external circuit information between two communication switch modules (210,310,410) is time division multiplexed onto the switch buses (101,102) such that the information transfers between all switch modules (210,310,410) takes place over the same two switch buses (101,102) but at separate predetermined time intervals such that at any one time interval within a predetermined cyclic time period only two switch modules (210,310,410) have access to the said switch buses (101,102) but over one complete cyclic time period all switch modules (210,310,410), for which an external circuit transfer is allocated have access to the said switch buses (101,102), each at its own predetermined transfer time interval.

8. A switching system as claimed in claim 7. whereby a common pair of switch buses (101,102) are time division multiplexed in discrete timing intervals and such timing intervals are are defined as time interval for the transfer of external circuit information between switch modules (210,310,410).

9. A switching system as claimed in any previous claim wherein each switching means (210,310,410) is coupled to the switch bus medium (101,102) by digital tristate logic circuits (216,217) which have the physical logic states of on, off and high impedance or disconnected.

10. A switching system as claimed in any preceding claim wherein the said timing and control module (110) comprises a microcomputer (111) and other digital logic circuits for the purpose of providing timing and control signals to the said switch modules (210,310,410).

11. A method of switching the information as represented by electrical signals on attached external circuits as claimed in any one of claims 1 to 10 wherein

time sampling of the external circuit electrical signals and the transfer of such time sampled information, or a representation thereof, between two such external circuits at discrete but periodic time intervals provides the means by which a logical connection can be established between two external circuits without the requirement for an actual time continuous physical connection to be established.

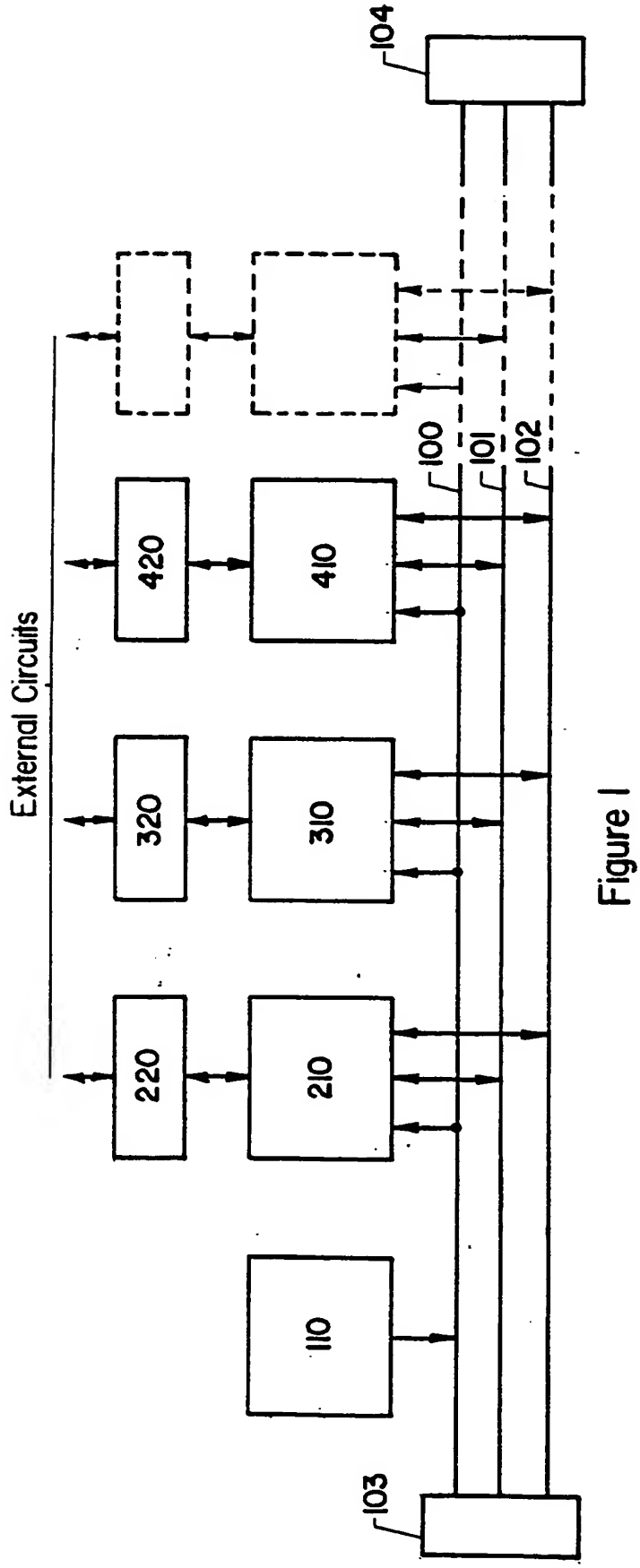

Figure 1

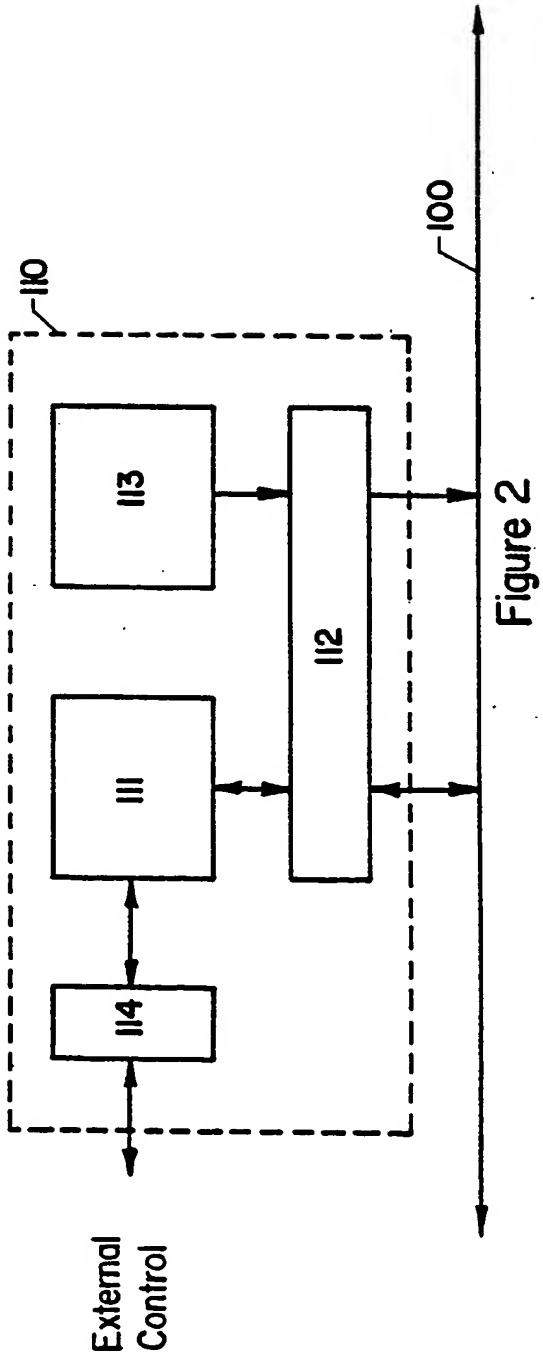

Figure 2

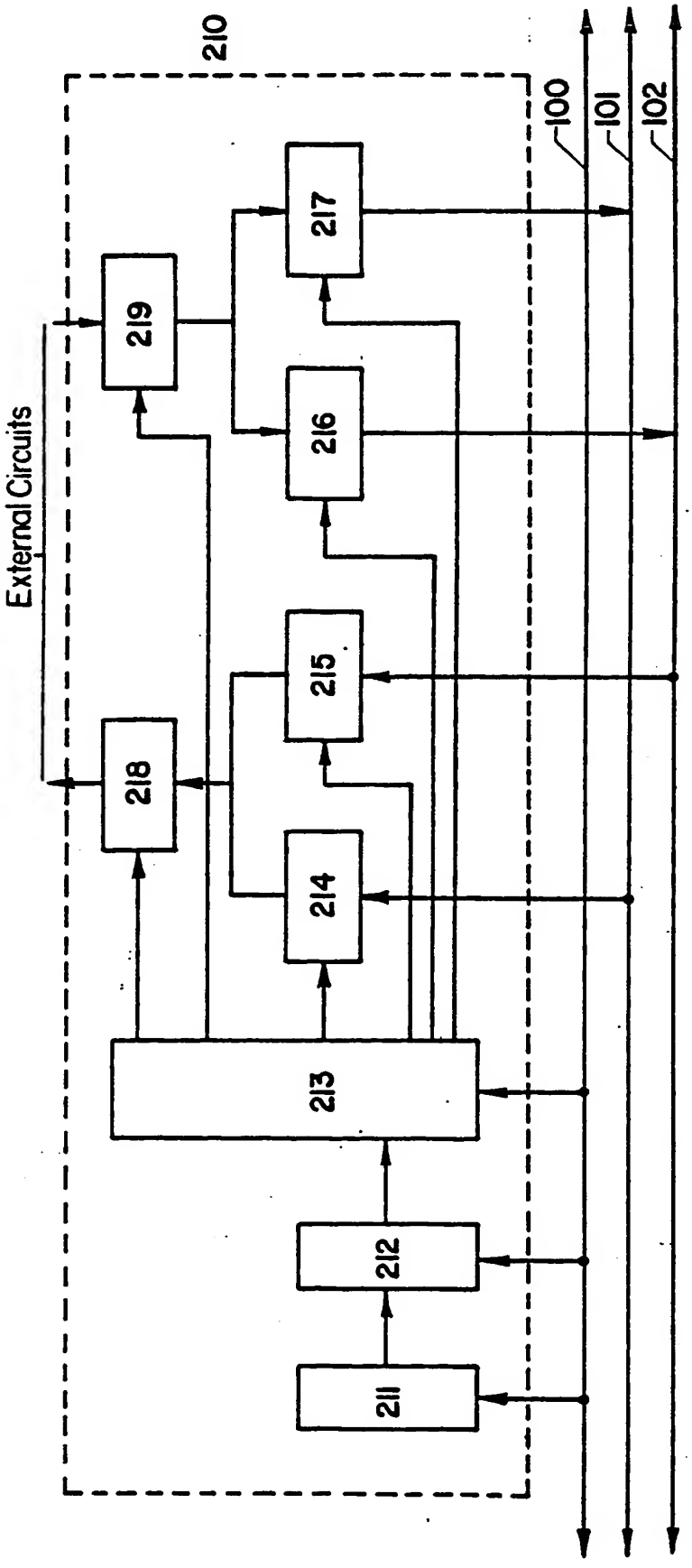

Figure 3

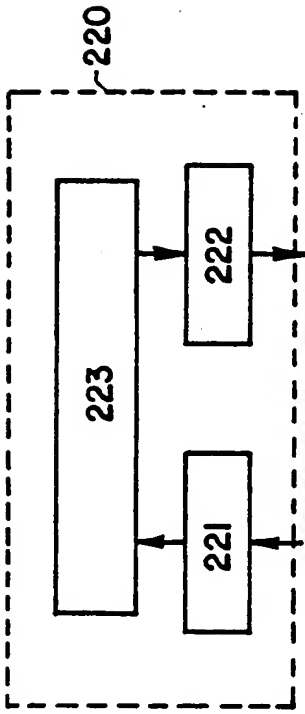

Figure 4

INTERNATIONAL SEARCH REPORT

International Application No PCT/AU 86/00149

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl.[4] H04Q 3/52, 11/00

II FIELDS SEARCHED

Minimum Documentation Searched

Classification System	Classification Symbols
IPC	H04Q 3/52, 11/00

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched

III. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
X	US, A, 4470139 (MUNTER) 12 April 1985 (12.04.85) See column 1 line 58 to column 2 line 29, column 4 line 11 to column 7 line 16, figures 3, 4.	1-11
A	US, A, 4201890 (LAWRENCE et al) 6 May 1980 (06.05.80)	
A	US, A, 4142068 (CHARRANSOL et al) 27 February 1979 (27.02.79)	
A	US, A, 4136263 (WILLIAMS) 23 January 1979 (23.01.79)	
A	US, A, 4105876 (FARRELL et al) 8 August 1978 (08.08.78)	
A	US, A, 4034159 (BURON) 5 July 1977 (05.07.77)	
A	US, A, 4022982 (HEMDAL) 10 May 1977 (10.05.77)	
A	US, A, 3892925 (FISK et al) 1 July 1975 (01.07.75)	

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IV CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
8 August 1986 (08.08.86)	26 AUGUST 1986 (26.08.86.)
International Searching Authority	**Signature of Authorized Officer**
AUSTRALIAN PATENT OFFICE	J. I. Cuthbert

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ANNEX TO THE INTERNATIONAL SEARCH REPORT ON
INTERNATIONAL APPLICATION NO. PCT/AU **86/00149**

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Patent Document Cited in Search Report	Patent Family Members		
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US 4142068	BE 855920 GB 1543482 SE 7707160	DE 2728078 IT 1079067	FR 2356322 NL 7706817
US 4022982	AU 87719/75 DE 2557175 IT 1062430	BE 836733 FR 2295667 JP 51088111	CA 1067987 GB 1525127 NL 7514856
US 3892925	AU 80451/75 CA 1035451 DE 2559770 IT 1037484 NL 7506531	BE 828615 CH 582449 FR 2273434 IT 1038272 SE 7505826	BR 7503473 DE 2523398 GB 1489285 JP 51000815
US 4105876	CA 1097784	DE 2743659	IT 1092823
US 4201890	AT 1867/79 BR 7901669 DE 2909762 ES 478734 GB 2016866 MX 146286 NZ 189850 SE 7902267 YU 654/79	AU 45016/79 CA 1132233 DK 1081/79 FI 790836 HK 193/84 NL 7902011 PL 214207 SE 8600184 ZA 7900941	BE 874930 CH 646828 EG 13657 FR 2420264 IN 152154 NO 790850 PT 69347 TR 20663
US 4136263	AU 61313/73 DE 2351133 IT 998744 NL 7314118	BE 806010 FR 2203239 JP 49094215 ZA 7307860	CA 1036277 GB 1410508 LU 68590